

**REMARKS/ARGUMENTS**

Claims 1-3, 5-6, 10-12, 14-15, and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno et al., U.S. Patent No. 6,370,494 in view of Hellestrand et al., U.S. Patent No. 6,230,114.

Claim 1 has been amended to more clearly recite producing “a system model comprising at least a first portion and a second portion” where simulation occurs at “a first accuracy level for at least a first portion of code comprising the first portion of the system model” and simulation occurs at “a second accuracy level different from the first accuracy level for at least a second portion of code comprising the second portion of the system model.” See also independent claim 10.

Mizuno et al. do not show “a first accuracy level” or “a second accuracy level” when they run a simulation. Hellestrand et al. show using a hardware simulator, “Thus where greater timing accuracy is required or desired than provided by running the user program completely on the host computer system, those aspects of the target processor's execution where greater accuracy is required may be modeled in hardware. Such hardware is then included in the digital circuitry simulated by the hardware simulator.” *Col. 35, lines 7-12*. Hellestrand et al., however, do not show simulation occurs at “a second accuracy level different from the first accuracy level for at least a second portion of code comprising the second portion of the system model.”

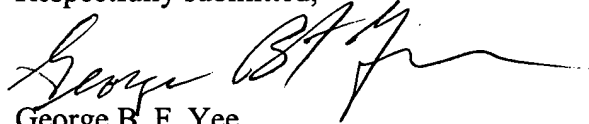
For at least the foregoing reasons, the Section 103 rejection of the claims is believed to be overcome.

**CONCLUSION**

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

  
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